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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

IE-703089-MC-EM1

In-Circuit Emulator Option Board

Target Devices

V850/SC1™

V850/SC2™

V850/SC3™

Document No. U15776EJ1V0UM00 (1st edition)

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INTRODUCTION

Target Readers	This manual is intended for users who design and develop application systems using the V850/SC1, V850/SC2, and V850/SC3.								
Purpose	The purpose of this manual is to describe the proper operation of the IE-703089-MC-EM1 and its basic specifications.								
Organization	<p>This manual is divided into the following parts.</p> <ul style="list-style-type: none">• Overview• Names and functions of components• Cautions								
How to Read This Manual	<p>It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.</p> <p>The IE-703089-MC-EM1 is used connected to the IE-703002-MC in-circuit emulator. This manual explains the basic setup procedure and switch settings of the IE-703002-MC when it is connected to the IE-703089-MC-EM1. For the names and functions of parts, and the connection of elements, refer to the IE-703002-MC User's Manual (U11595E).</p> <p>To learn about the basic specifications and operation methods → Read this manual in the order of the CONTENTS.</p> <p>To learn the operation methods and command functions, etc., of the IE-703002-MC and IE-703089-MC-EM1 → Read the user's manual of the debugger (sold separately) that is used.</p>								
Conventions	<p>Note: Footnote for item marked with Note in the text</p> <p>Caution: Information requiring particular attention</p> <p>Remark: Supplementary information</p> <p>Numeral representation: Binary ... xxxx or xxxxB Decimal ... xxxx Hexadecimal ... xxxxH</p> <p>Prefix indicating the power of 2 (address space, memory capacity): K (kilo): $2^{10} = 1024$ M (mega): $2^{20} = 1024^2$</p>								
Terminology	<p>The meanings of terms used in this manual are listed below.</p> <table><tr><td>Emulation CPU</td><td>The CPU that executes the program prepared by the user in the emulator.</td></tr><tr><td>Target device</td><td>The device that is targeted for emulation.</td></tr><tr><td>Target system</td><td>The system (user-built system) that is targeted for debugging. This includes the target program and user-configured hardware.</td></tr><tr><td>IE system</td><td>The combination of the IE-703002-MC and IE-703089-MC-EM1</td></tr></table>	Emulation CPU	The CPU that executes the program prepared by the user in the emulator.	Target device	The device that is targeted for emulation.	Target system	The system (user-built system) that is targeted for debugging. This includes the target program and user-configured hardware.	IE system	The combination of the IE-703002-MC and IE-703089-MC-EM1
Emulation CPU	The CPU that executes the program prepared by the user in the emulator.								
Target device	The device that is targeted for emulation.								
Target system	The system (user-built system) that is targeted for debugging. This includes the target program and user-configured hardware.								
IE system	The combination of the IE-703002-MC and IE-703089-MC-EM1								

Related Documents

When using this manual, refer to the following manuals.

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

○ Documents related to development tools (user's manuals)

Document Name		Document Number
IE-703002-MC In-circuit emulator		U11595E
IE-703089-MC-EM1 In-circuit emulator option board		This manual
CA850 C Compiler package Ver. 2.40	Operation	To be prepared
	C Language	U16054E
	PM Plus	To be prepared
	Assembly Language	U16042E
ID850 Integrated debugger Ver.2.40	Operation Windows™ based	U15181E
SM850 System simulator Ver.2.40	Operation Windows based	U15182E
SM850 System simulator Ver.2.00 or later	External Part User Open Interface Specifications	U14873E
RX850 Real-time OS Ver.3.13 or later	Basics	U13430E
	Installation	U13410E
	Technical	U13431E
RX850 Pro Real-time OS Ver.3.13	Basics	U13773E
	Installation	U13774E
	Technical	U13772E
RD850 Task debugger Ver.3.01		U13737E
RD850 Pro Task debugger Ver.3.01		U13916E
AZ850 System performance analyzer Ver.3.0		U14410E
PG-FP4 Flash Memory Programmer		U15260E

CONTENTS

CHAPTER 1 OVERVIEW	10
1.1 Hardware Configuration	10
1.2 Features (When Connected to IE-703002-MC)	11
1.3 Function Specifications (When Connected to IE-703002-MC)	11
1.4 System Configuration	12
1.5 Contents in Carton	13
1.6 Connection Between IE-703002-MC and IE-703089-MC-EM1	15
 CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS	 19
2.1 Component Names and Functions of IE-703089-MC-EM1	20
2.2 Clock Settings	23
2.2.1 Main clock setting	23
2.2.2 Subclock setting	24
2.3 Illegal Access Detection ROM Setting	25
2.4 CPU Operation Voltage Range Switching Setting	25
2.5 Address Output Setting of Separate Bus	26
 CHAPTER 3 FACTORY SETTINGS	 27
 CHAPTER 4 CAUTIONS	 28
4.1 V _{DD} and PORTV _{DD} of Target System	28
4.2 I/O Signal	29
4.3 V _{PP} Signal	29
4.4 NMI Signal Mask Function	29
 CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICE AND TARGET INTERFACE CIRCUIT	 30
 APPENDIX PACKAGE DRAWINGS	 33

LIST OF FIGURES

Figure No.	Title	Page
1-1	System Configuration	12
1-2	Contents in Carton	13
1-3	Accessories	14
1-4	Connection Between IE-703002-MC and IE-703089-MC-EM1	16
1-5	Connection of IE-703089-MC-EM1 and SWEX-144SD-1	18
2-1	IE-703089-MC-EM1	20
2-2	SW5	26
4-1	Schematic Diagram of Power Supply Acquisition	28
4-2	I/O Signal Flow Path	29
5-1	Equivalent Circuit of Emulation Circuit.....	31

LIST OF TABLES

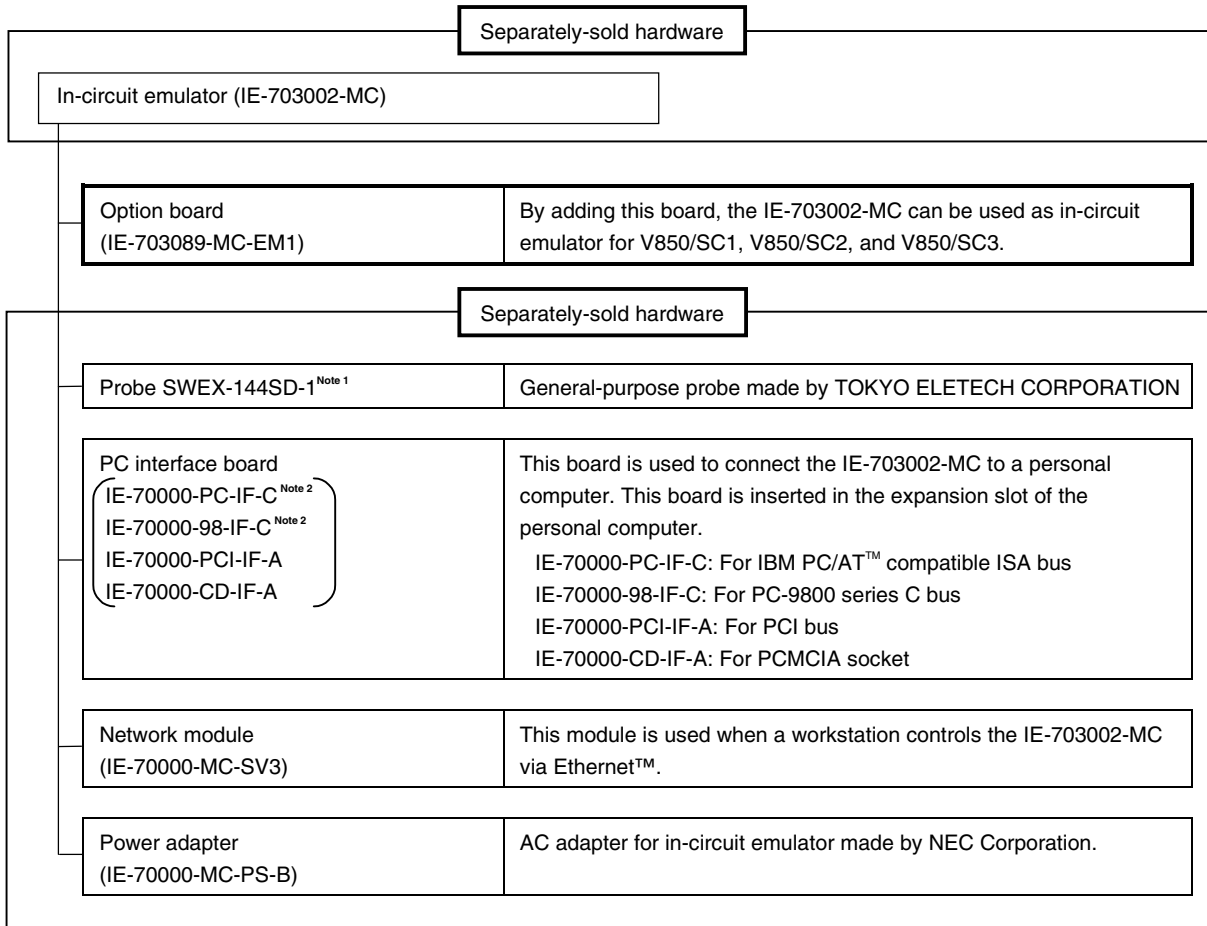
Table No.	Title	Page
2-1	Main Clock Setting.....	23
2-2	Subclock Setting.....	24
2-3	JP1 Setting in IE-703002-MC	25
2-4	JP3 and JP4 Setting in IE-703002-MC	25
2-5	SW5 Setting.....	26

CHAPTER 1 OVERVIEW

The IE-703089-MC-EM1 is an option board for the IE-703002-MC in-circuit emulator. By connecting the IE-703089-MC-EM1 and IE-703002-MC, hardware and software can be debugged efficiently in system development using the V850/SC1, V850/SC2, and V850/SC3.

In this manual, the basic setup procedure and switch settings of the IE-703002-MC when the IE-703089-MC-EM1 is connected are described. For the names and functions of the parts of the IE-703002-MC, and for the connection of elements, refer to the **IE-703002-MC User's Manual (U11595E)**.

1.1 Hardware Configuration



- Notes**
1. For further information, contact Daimaru Kogyo Co., Ltd.
Tokyo Electronics Department (TEL +81-3-3820-7112)
Osaka Electronics Department (TEL +81-6-6244-6672)
 2. Cannot be used for PC98-NX series

1.2 Features (When Connected to IE-703002-MC)

- Maximum operating frequency: 20 MHz (at 5.0 V operation)
- The following pins can be masked.
RESET, NMI, WAIT, HLDRQ
- External bus interface
- Connected to target system via following method:
 - Attach a probe (sold separately) to the pod tip for connection
- The dimensions of the IE-703089-MC-EM1 are as follows.

Parameter		Value
Power consumption (max. value at 5.0 V supply voltage)		2.5 W (at 20 MHz operation frequency) ^{Note}
External dimensions (Refer to APPENDIX PACKAGE DRAWINGS)	Height	50 mm
	Length	180 mm
	Width	250 mm
Weight		300 g

Note 12.5 W when the IE-703002-MC is connected to the IE-703089-MC-EM1

1.3 Function Specifications (When Connected to IE-703002-MC)

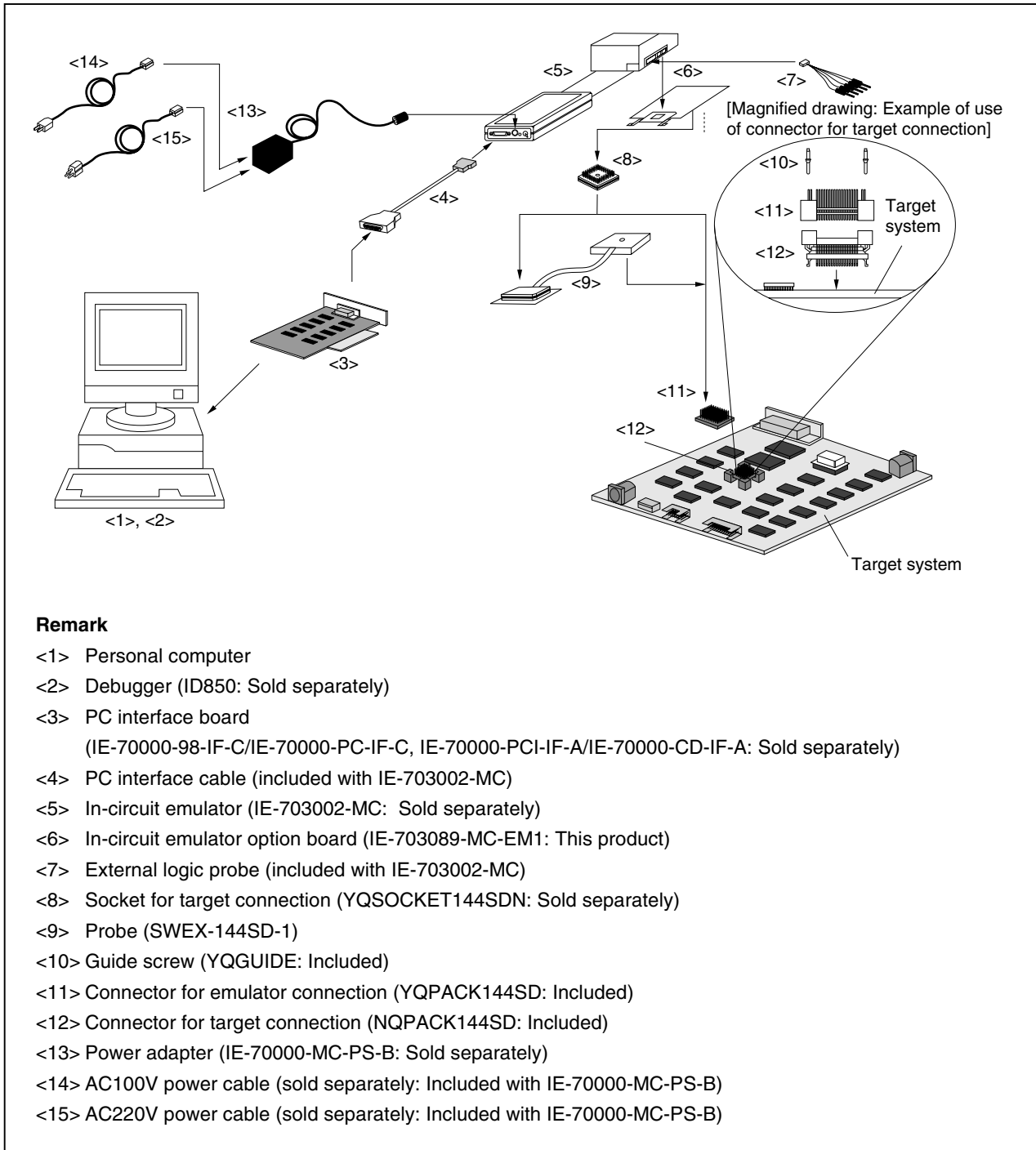
Parameter			Specification
Emulation memory capacity	Internal ROM		512 KB
	External memory	In ROMless mode	2 MB
		When using iROM	1 MB
Coverage memory capacity for execution/pass detection	Internal ROM		512 KB
	External memory	In ROMless mode	2 MB
		When using iROM	1 MB
Coverage memory capacity for memory access detection	External memory		1 MB
Coverage memory capacity for branching entry number counting	Internal ROM		512 KB
	External memory	In ROMless mode	2 MB
		When using iROM	1 MB
Trace memory capacity			150 bits × 32 K frames
Time measurement function			Measurement possible by time tag or 3 timers
External logic probe			4-bit external trace possible
			Event setting of trace/break possible
Break function			Event break
			Step execution break
			Forcible break
			Fail safe break <ul style="list-style-type: none">• Illegal access to peripheral I/O• Access to guard space• Write to ROM space

Caution Some of the functions may not be supported, depending on the debugger used.

1.4 System Configuration

The system configuration when connecting the IE-703002-MC to the IE-703089-MC-EM1 and a personal computer is shown below.

Figure 1-1. System Configuration

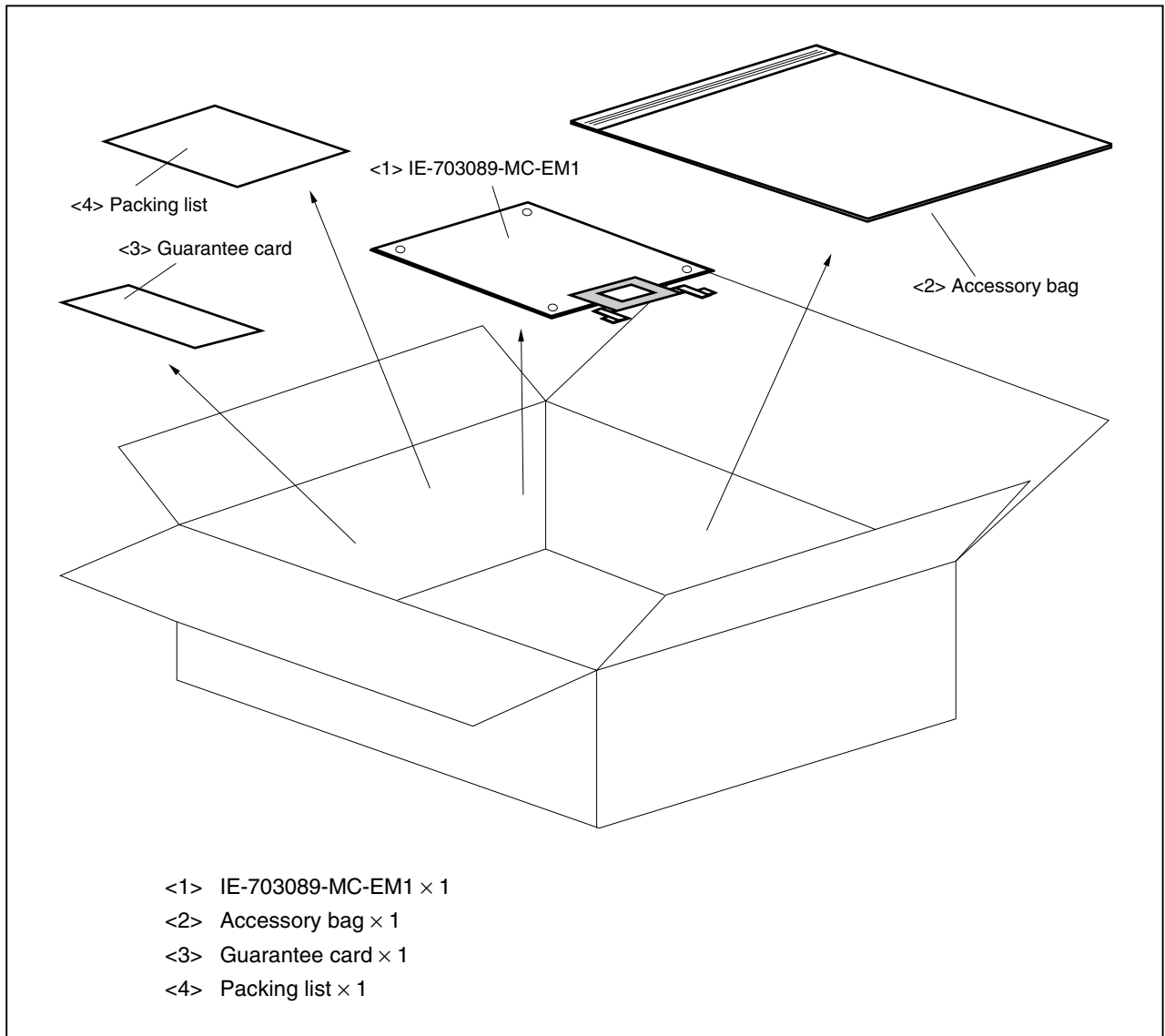


1.5 Contents in Carton

The carton of the IE-703089-MC-EM1 contains the main unit, guarantee card, packing list, and accessory bag. Make sure that the accessory bag contains this manual and the connector accessories. If there are missing or damaged items, please contact an NEC sales representative or an NEC distributor.

Return the guarantee card included in the carton after filling in all the items.

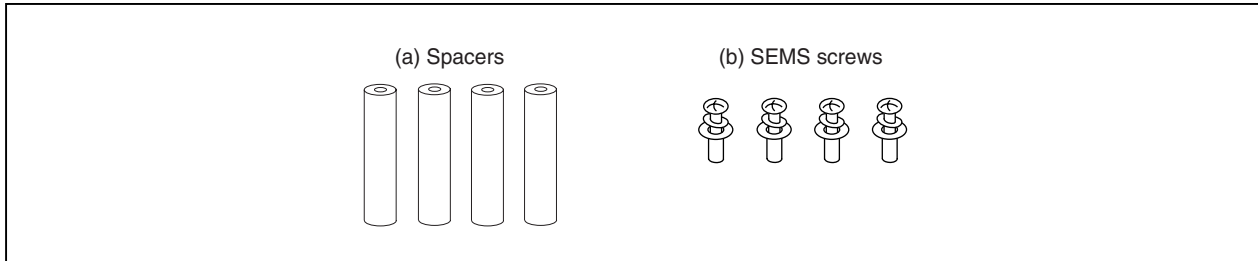
Figure 1-2. Contents in Carton



Check that the accessory bag contains this manual, an accessory list (× 1), and the following accessories.

- (a) Spacers × 4
- (b) SEMS screws × 4

Figure 1-3. Accessories



1.6 Connection Between IE-703002-MC and IE-703089-MC-EM1

The procedure for connecting the IE-703002-MC and IE-703089-MC-EM1 is described below.

Caution **Connect carefully so as not to break or bend connector pins.**

- <1> Remove the pod cover (lower) of the IE-703002-MC.
- <2> Set the PGA socket lever of the IE-703089-MC-EM1 to the OPEN position as shown in Figure 1-4 (b).
- <3> Connect the IE-703089-MC-EM1 to the PGA socket at the back of the IE-703002-MC pod (refer to Figure 1-4 (c)). When connecting, position the IE-703002-MC and IE-703089-MC-EM1 so that they are horizontal.
- <4> Set the PGA socket lever of the IE-703089-MC-EM1 to the CLOSE position as shown in Figure 1-4 (b).
- <5> When connecting the probe (SWEX-144SD-1) to the IE-703089-MC-EM1, attach it to CN1 on the rear of the IE-703089-MC-EM1, aligning each pin 1 (refer to **Figure 1-5**).
- <6> Place the supplied spacers in the four corner holes of the IE-703089-MC-EM1. Fix the spacers with the supplied SEMS screws.
- <7> Fix the IE-703002-MC pod cover (upper) with nylon rivets.

Figure 1-4. Connection Between IE-703002-MC and IE-703089-MC-EM1 (1/2)

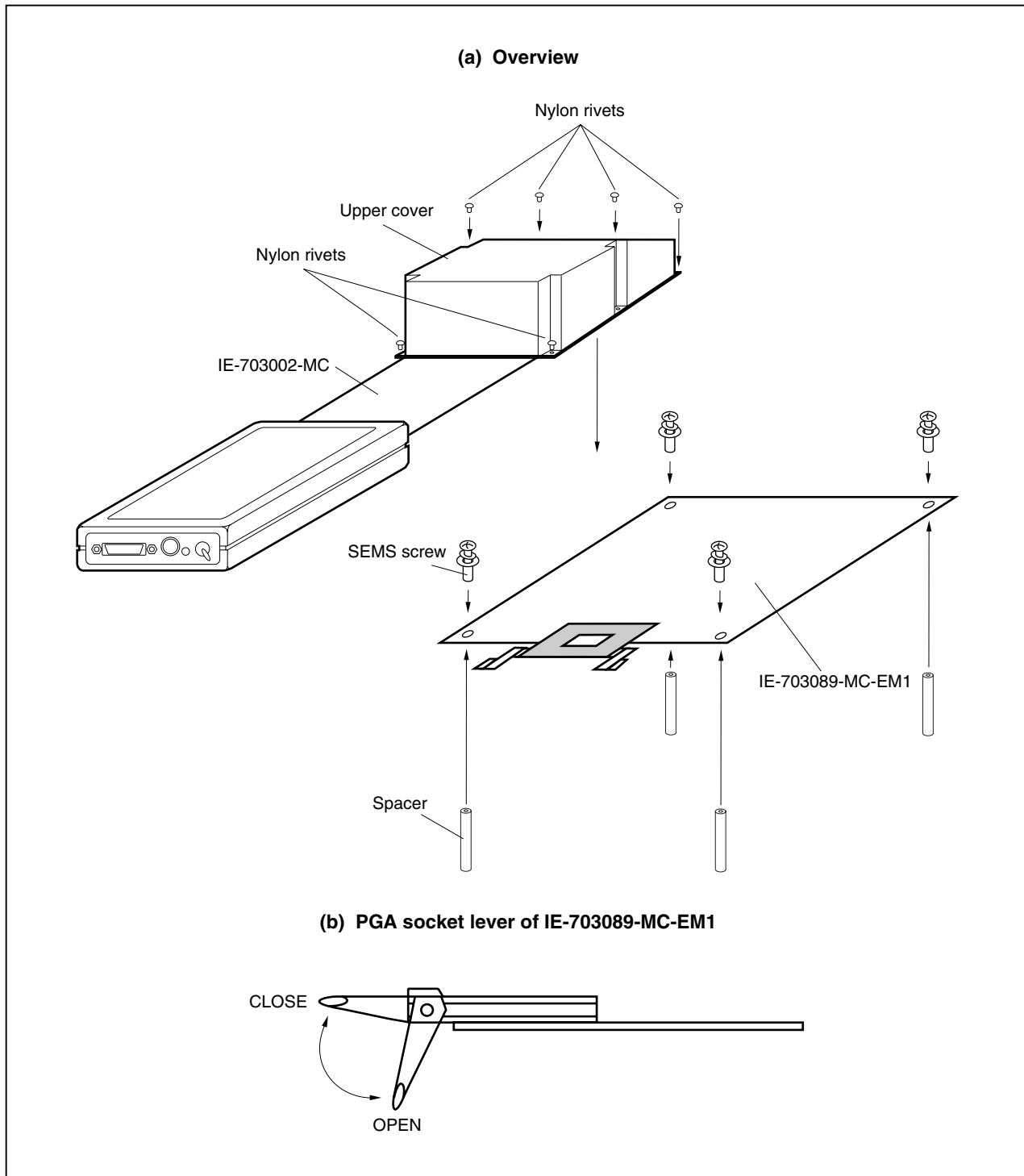


Figure 1-4. Connection Between IE-703002-MC and IE-703089-MC-EM1 (2/2)

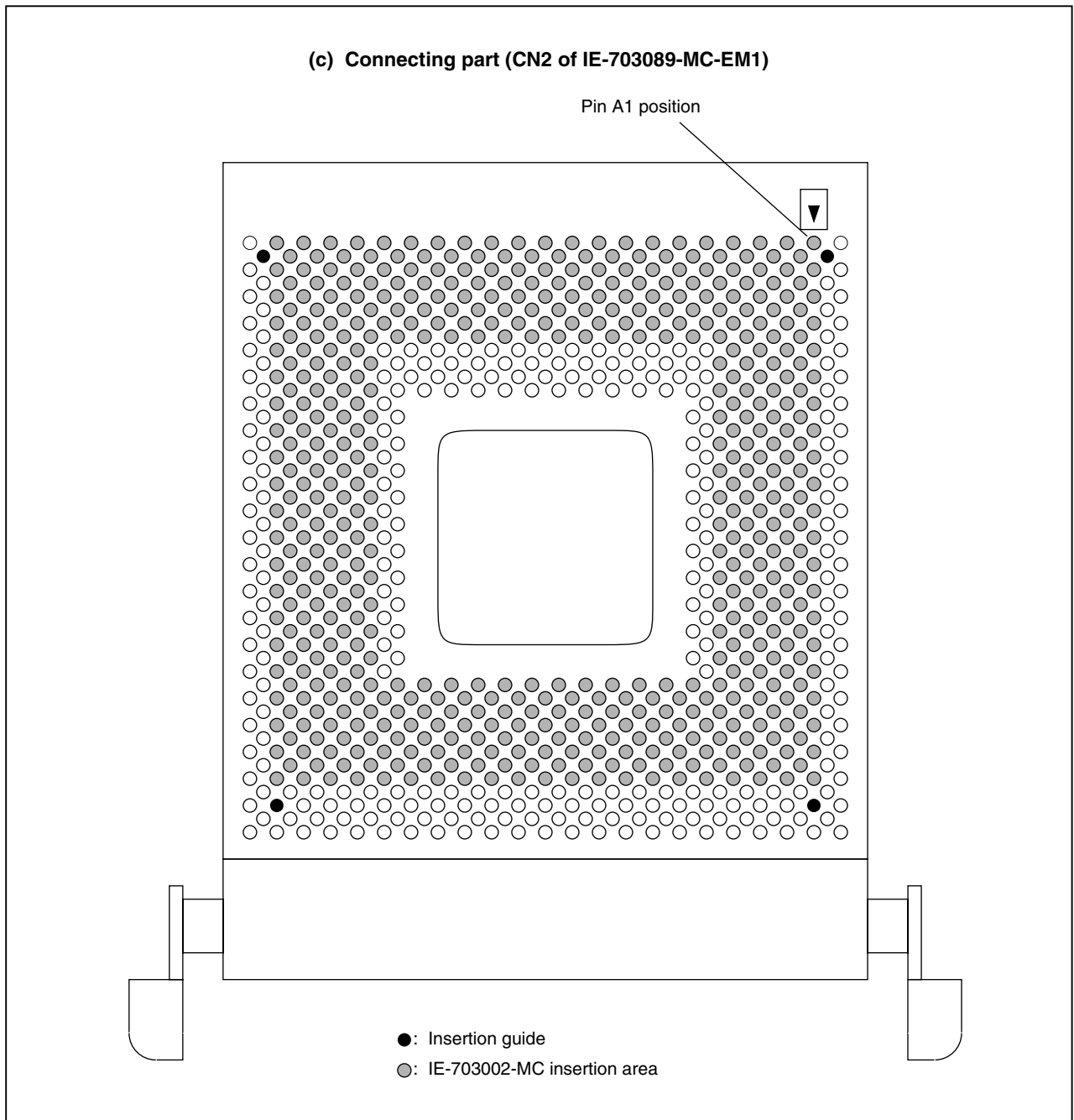
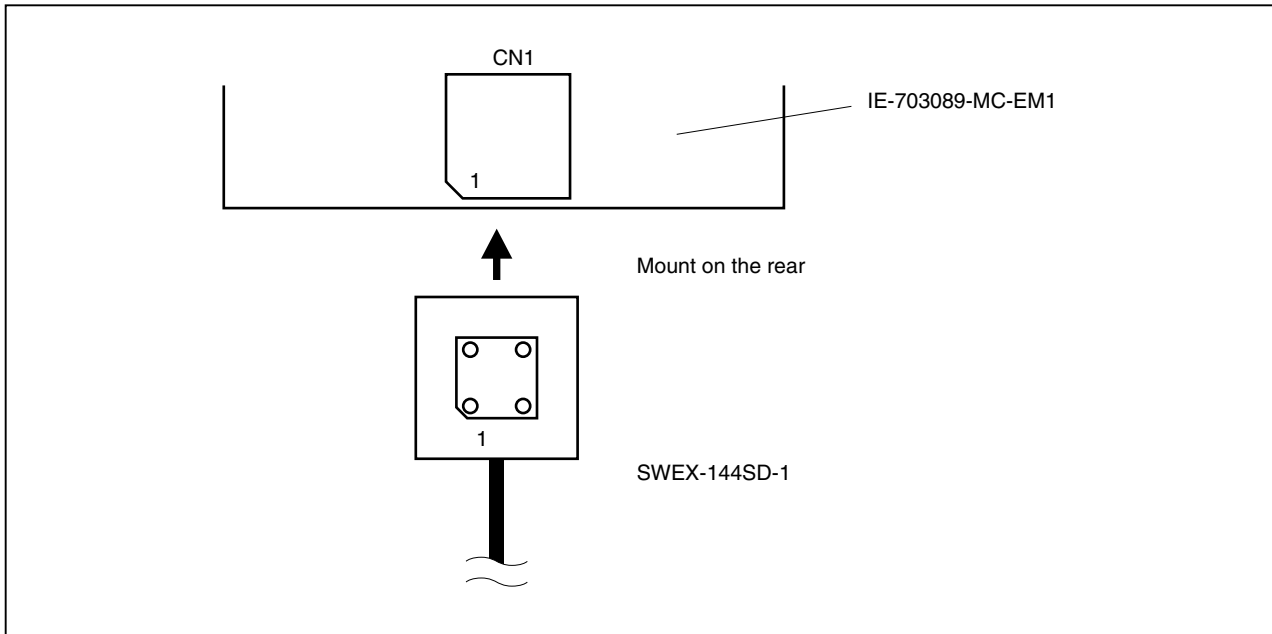


Figure 1-5. Connection of IE-703089-MC-EM1 and SWEX-144SD-1



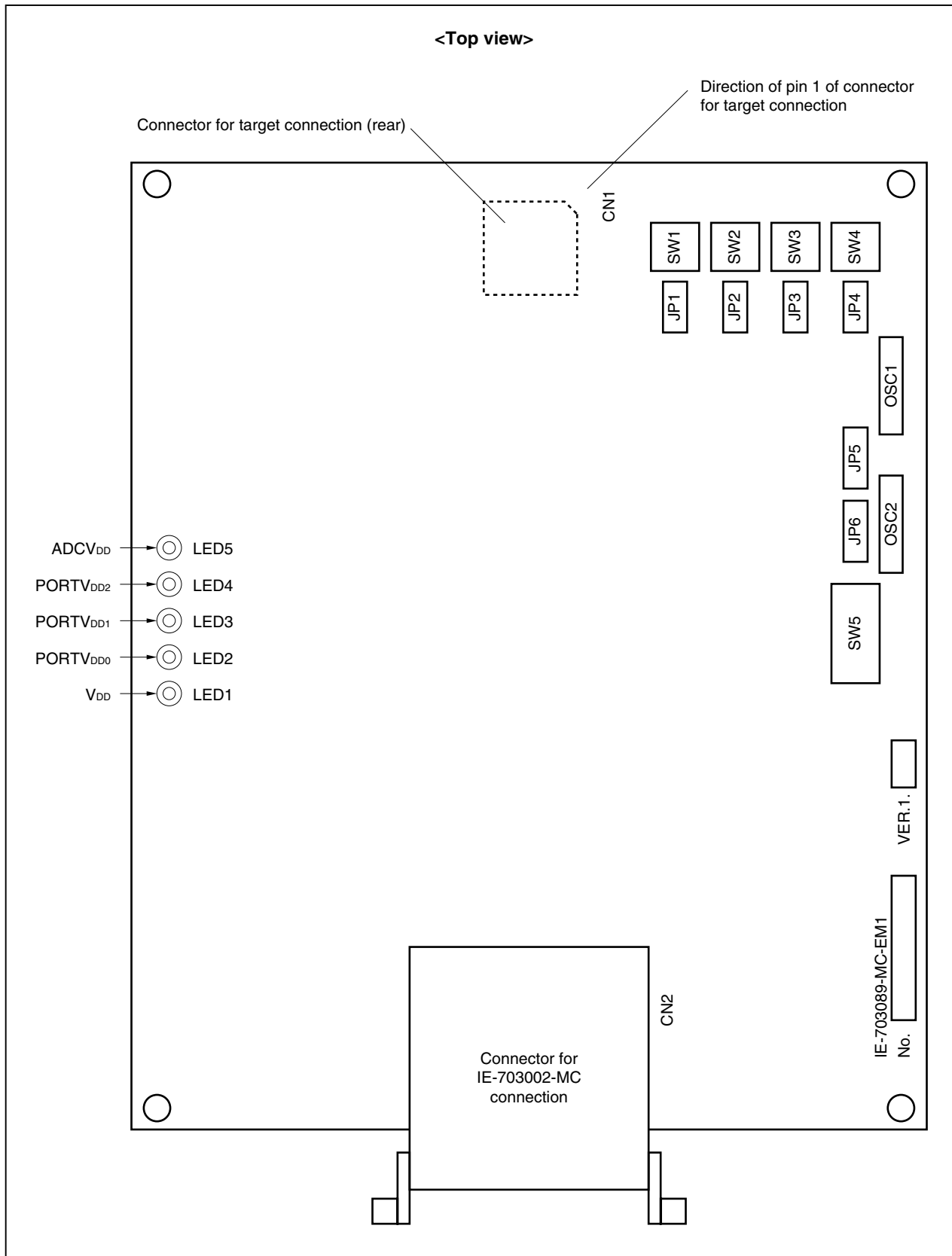
CHAPTER 2 NAMES AND FUNCTIONS OF COMPONENTS

This chapter describes the names, functions, and switch settings of components in the IE-703089-MC-EM1.

For the details of the pod, jumper, and switch positions, etc., refer to the **IE-703002-MC User's Manual (U11595E)**.

2.1 Component Names and Functions of IE-703089-MC-EM1

Figure 2-1. IE-703089-MC-EM1



(1) OSC1

OSC1 is a socket for the main clock crystal oscillator and for mounting capacitors. (For details, refer to **2.2.1 Main clock setting**).

(2) JP5

JP5 is a jumper to switch the main clock supply source. (For details, refer to **2.2.1 Main clock setting**.)

(3) OSC2

OSC2 is a socket for the main clock crystal oscillator and for mounting capacitors. (For details, refer to **2.2.2 Subclock setting**.)

(4) JP6

JP6 is a jumper to switch the subclock supply source. (For details, refer to **2.2.2 Subclock setting**.)

(5) JP1

Reserved. Use this jumper with the factory setting (2-3 shorted).

(6) SW1

Reserved. Use this switch with the factory setting (3-6 side).

(7) JP2

Reserved. Use this jumper with the factory setting (2-3 shorted).

(8) SW2

Reserved. Use this switch with the factory setting (3-6 side).

(9) JP3

Reserved. Use this jumper with the factory setting (2-3 shorted).

(10) SW3

Reserved. Use this switch with the factory setting (3-6 side).

(11) JP4

Reserved. Use this jumper with the factory setting (2-3 shorted).

(12) SW4

Reserved. Use this switch with the factory setting (3-6 side).

(13) SW5

SW5 is a switch to output the addresses (A1 to A15) of the separate bus. (For details, refer to **2.5 Address Output Setting of Separate Bus**.)

(14) LED1 to LED5

Lit: Power is supplied by the target system.

Not lit: Power is supplied by the power supply inside the emulator.

LED1: V_{DD}

LED2: $PORTV_{DD0}$

LED3: $PORTV_{DD1}$

LED4: $PORTV_{DD2}$

LED5: $ADCV_{DD}$

(15) Connector for IE-703002-MC connection (CN2)

CN2 is a connector to connect the IE-703089-MC-EM1 to the IE-703002-MC.

(16) Connector for target connection (CN1)

CN1 is a connector to connect the IE-703089-MC-EM1 to the probe.

2.2 Clock Settings

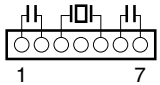
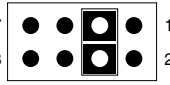
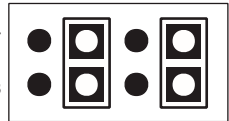
This section describes the clock settings.

For the position of OSC1 and JP5 in the IE-703089-MC-EM1, refer to **Figure 2-1**.

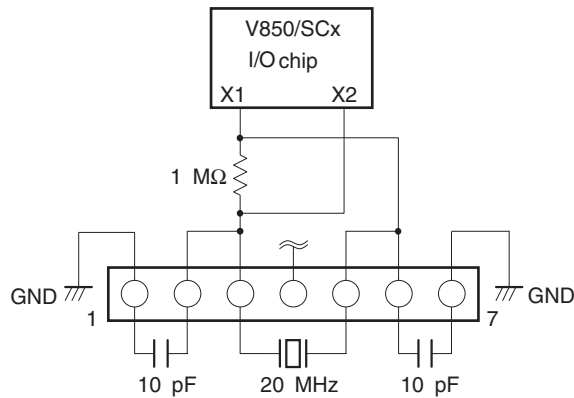
For the jumper and switch positions in the IE-703002-MC, refer to the **IE-703002-MC User's Manual (U11595E)**.

2.2.1 Main clock setting

Table 2-1. Main Clock Setting

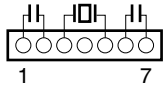
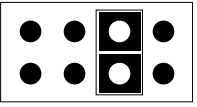
Emulator Usage Environment	Clock Supply Method	IE-703089-MC-EM1 Setting		IE-703002-MC Setting		
		OSC1	JP5	SW1	SW2	JP2
When using emulator as standalone unit	Internal clock			ON	OFF	
When using emulator with target system	Internal clock	(Oscillator mounted)	(3-4 shorted: Fixed)			

Caution Emulation cannot be performed by inputting a clock from the target system.
The specifications of OSC1 are as follows.

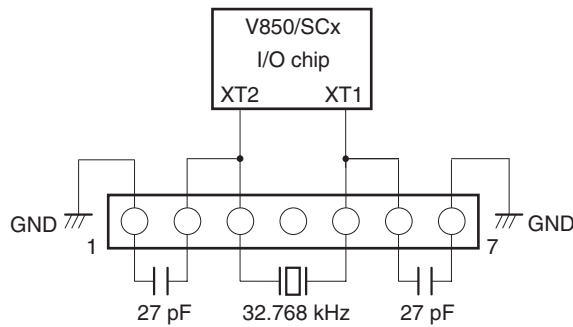


2.2.2 Subclock setting

Table 2-2. Subclock Setting

Emulator Usage Environment	Clock Supply Method	IE-703089-MC-EM1 Setting	
		OSC2 ^{Note 2}	JP6
When using emulator as standalone unit	Internal clock ^{Note 1}	 (Oscillator mounted)	 (3-4 shorted: Fixed)
When using emulator with target system	Internal clock ^{Note 1}		

- Notes**
1. A clock input by an oscillator cannot be used for the internal clock.
 2. To use a subclock frequency other than 32.768 kHz, remove the resonator on OSC2 and mount an oscillator.
The specifications of OSC2 are as follows.

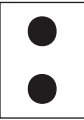


Caution Emulation cannot be performed by inputting a clock from the target system.

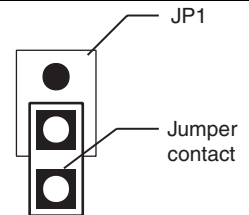
2.3 Illegal Access Detection ROM Setting

If using the IE-703002-MC for an in-circuit emulator for the V850/SCx by connecting the IE-703089-MC-EM1, set JP1 of the IE-703002-MC as follows.

Table 2-3. JP1 Setting in IE-703002-MC

JP1		Description
Open ^{Note}		Illegal access detection ROM (mounted on IE-703089-MC-EM1) for V850/SCx is used.

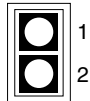
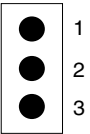
Note When JP1 is set to open, keep the removed jumper contact attached to one pin as shown in the drawing on the right.



2.4 CPU Operation Voltage Range Switching Setting

If using the IE-703002-MC for an in-circuit emulator for the V850/SCx by connecting the IE-703089-MC-EM1, set JP3 and JP4 of the IE-703002-MC as follows.

Table 2-4. JP3 and JP4 Setting in IE-703002-MC

JP3, JP4		Description
JP3	 (Shorted)	The operation voltage range of the IE-703002-MC is 3.0 to 5.5 V.
JP4	 (Open)	The power supply for PORTV _{DD} is generated on the IE-703089-MC-EM1.

2.5 Address Output Setting of Separate Bus

When using the separate bus function while debugging using the IE-703089-MC-EM1, switching to the separate bus output function is not possible by setting the memory address output register (MAM) by software.

Use DIP switch SW5 to output the address of the separate bus function while debugging using the IE-703089-MC-EM1.

The switches of SW5 and their corresponding ports are shown in Table 2-5.

Figure 2-2. SW5

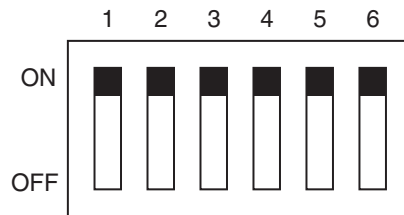
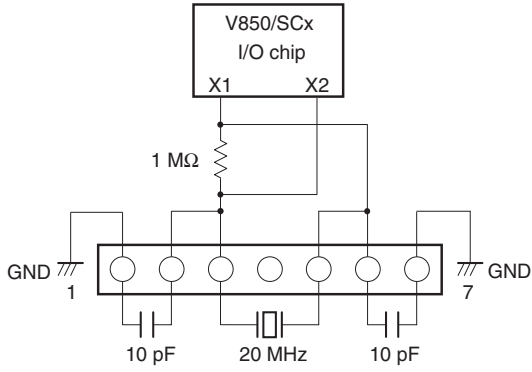
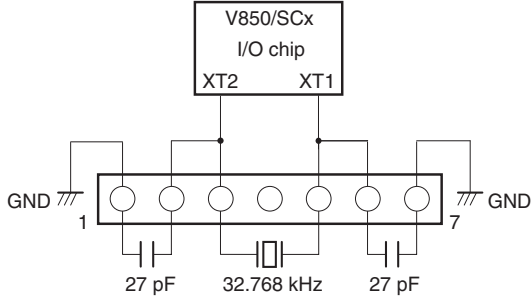
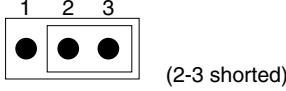
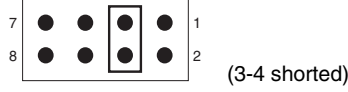
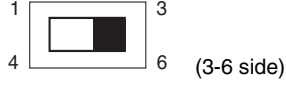
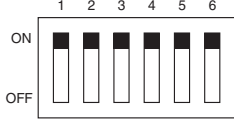


Table 2-5. SW5 Setting

Switch	Setting	Selection of Alternate-Function Pin
1	ON	P113 to P110 (port mode)
	OFF	A4 to A1 output to P113 to P110 (memory address output function of separate bus)
2	ON	P103 to P100 (port mode)
	OFF	A8 to A5 output to P103 to P100 (memory address output function of separate bus)
3	ON	P107 to P104 (port mode)
	OFF	A12 to A9 output to P107 to P104 (memory address output function of separate bus)
4	ON	P34 (port mode)
	OFF	A13 output to P34 (memory address output function of separate bus)
5	ON	P35 (port mode)
	OFF	A14 output to P35 (memory address output function of separate bus)
6	ON	P33 (port mode)
	OFF	A15 output to P33 (memory address output function of separate bus)

CHAPTER 3 FACTORY SETTINGS

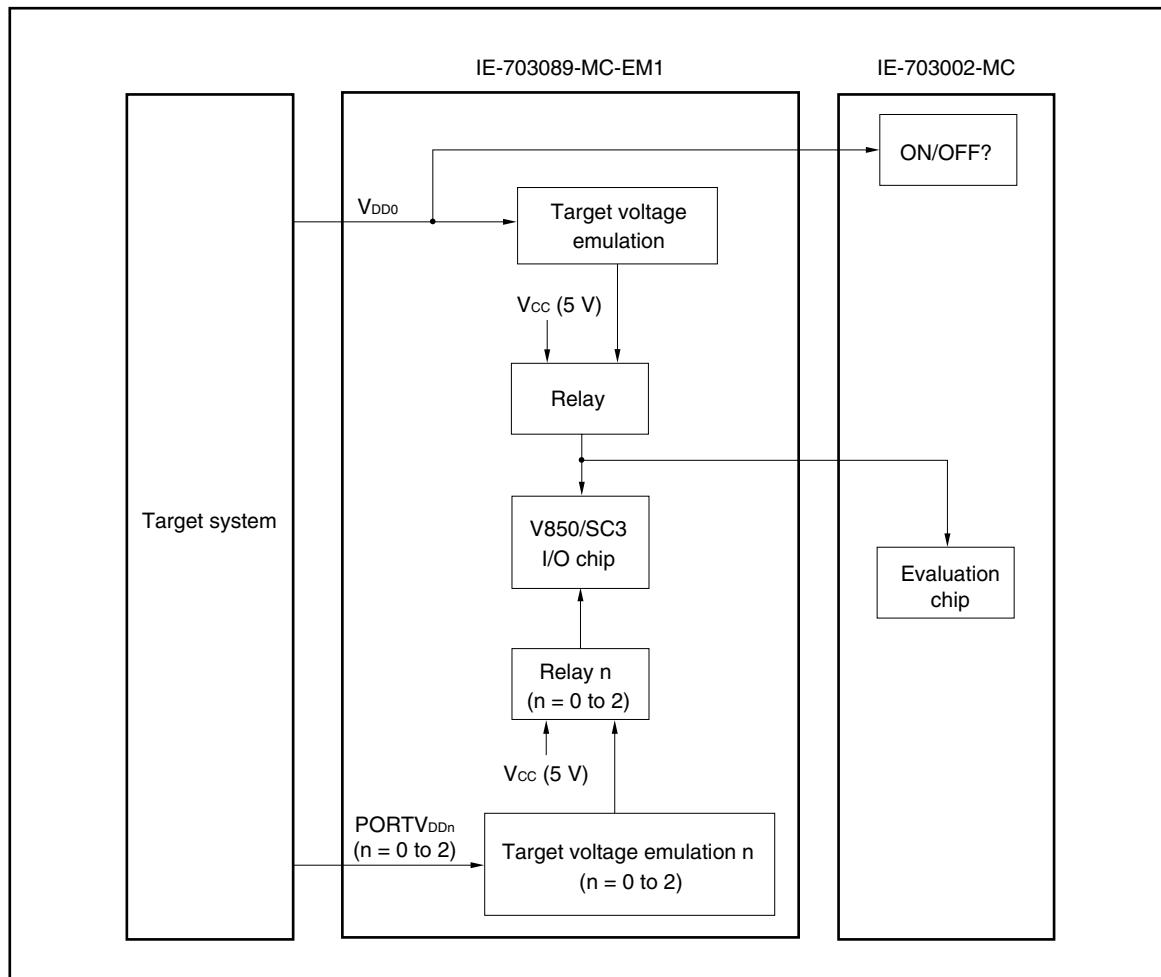
Item	Description	Remark
OSC1		Pins 1 and 2: For mounting capacitor (10 pF) Pins 6 and 7: For mounting capacitor (10 pF) Pins 3 to 5: Crystal oscillator (20 MHz) Pin 4: Open 20 MHz clock supplied for main clock
OSC2		Pins 1 and 2: For mounting capacitor (27 pF) Pins 6 and 7: For mounting capacitor (27 pF) Pins 3 to 5: Crystal oscillator (32.768 MHz) Pin 4: Open 32.768 MHz clock supplied for subclock
JP1 to JP4		Pins 2 and 3: Short Pin 1: Open Use these jumpers with the factory settings.
JP5, JP6		Pins 1 and 2: Open Pins 3 and 4: Shorted Pins 5 and 6: Open Pins 7 and 8: Open Use these jumpers with the factory settings.
SW1 to SW4		3-6 side Use these switches with the factory settings.
SW5		All bits ON (port mode)

CHAPTER 4 CAUTIONS

4.1 V_{DD} and $PORTV_{DDn}$ of Target System

- (1) V_{DD} in the target system is used to sense the level for target system power supply ON/OFF.
- When V_{DD} is lower than 3.5 V, it is judged that the target system is not connected, and mapping of the target memory cannot be performed with a debugger (FCAN cannot be used).
 - When V_{DD} is 3.5 V or higher, it is judged that the target system is connected, and mapping of the target memory can be performed with a debugger (FCAN can be used).
- (2) $PORTV_{DDn}$ ($n = 0$ to 2) in the target system is not supplied directly to the emulator chip; it is connected to the target voltage emulation circuit.
- When $PORTV_{DDn}$ is lower than 3.3 V, V_{CC} (5 V) in the internal emulator is supplied to the emulator chip.
 - When $PORTV_{DDn}$ is 3.3 V or higher, a voltage of the same potential as $PORTV_{DDn}$ in the target system is generated and supplied to the emulator chip.

Figure 4-1. Schematic Diagram of Power Supply Acquisition



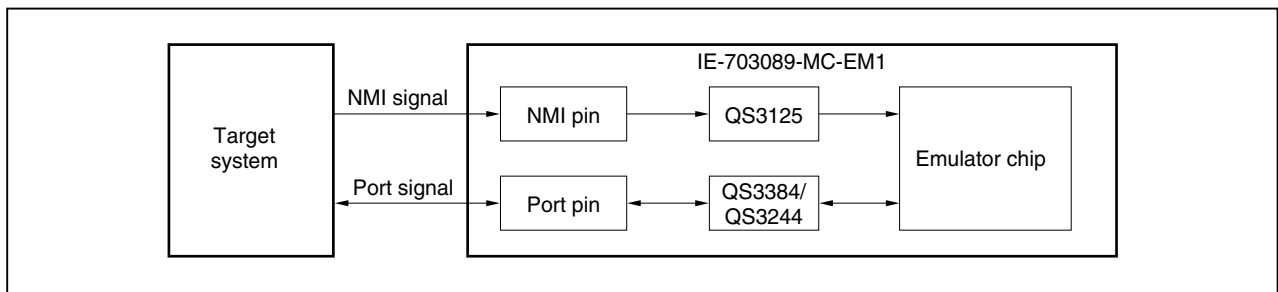
- (3) The V_{DD1} signal from the target system is left open in the IE-703089-MC-EM1.
- (4) The following conditions must be satisfied when other than $V_{DD0} = V_{DD1} = ADCV_{DD} = PORTV_{DD1} = PORTV_{DD2}$.
 1. When FCAN is used, $PORTV_{DD1} \leq PORTV_{DD2}$ (restricted by the power supply voltage conditions of the in-circuit emulator)
 2. When ADC is used, $V_{DD0} = ADCV_{DD} = 4.5$ to 5.5 V

4.2 I/O Signal

The input signal (NMI signal) from the target system, the I/O signals for ports 4, 5, 6, and 11, and the I/O signal for port 9 are all delayed ($t_{PD} = 0.25$ ns (typ.)) because they pass through Q switches QS3125, QS3384, and QS3244, respectively, before being input to the emulator chip.

The DC characteristics also change. The input voltage becomes $V_{IH} = 2.0$ V (MIN.), $V_{IL} = 0.8$ V (MAX.), and the input current becomes $I_{IN} = \pm 0.5$ μ A (MAX.).

Figure 4-2. I/O Signal Flow Path



4.3 V_{PP} Signal

The V_{PP} signal from the target system is left open in the emulator.

4.4 NMI Signal Mask Function

When using the P00/NMI pin in the port mode, do not mask the NMI signal.

CHAPTER 5 DIFFERENCES BETWEEN TARGET DEVICE AND TARGET INTERFACE CIRCUIT

Differences between the signal lines of the target device and the signal lines of the IE-703089-MC-EM1 target interface circuit are described in this chapter.

The target device is a CMOS circuit, whereas the target interface circuit of the IE-703089-MC-EM1 is configured with an emulation circuit such as a gate array TTL or CMOS-IC.

When debugging the IE system connected to the target system, the IE system emulates as if the real target device is operating on the target system.

Small differences occur however, because the IE system is emulating actual operation.

(1) Signals input/output to/from the emulation gate array

- P47 to P40
- P57 to P50
- P67 to P60
- P97 to P90
- P117 to P110
- P133 to P130

(2) Other signals

- P07 to P00
- P17 to P10
- P27 to P20
- P37 to P30
- P77 to P70
- P83 to P80
- P107 to P100
- P127 to P120
- P147 to P140
- P157 to P150
- P176 to P170
- V_{DD0}
- PORTV_{DD0}, PORTV_{DD1}, PORTV_{DD2}, ADCV_{DD}
- CLKOUT
- $\overline{\text{RESET}}$
- V_{DD1}
- MODE/V_{PP}
- CPUREG
- X1, X2, XT1, XT2
- GND0, GND1, GND2, PORTGND0, PORTGND1, ADCGND

Figure 5-1 shows the signals in (1) and (2) above in the circuit for the IE system.

Figure 5-1. Equivalent Circuit of Emulation Circuit (1/2)

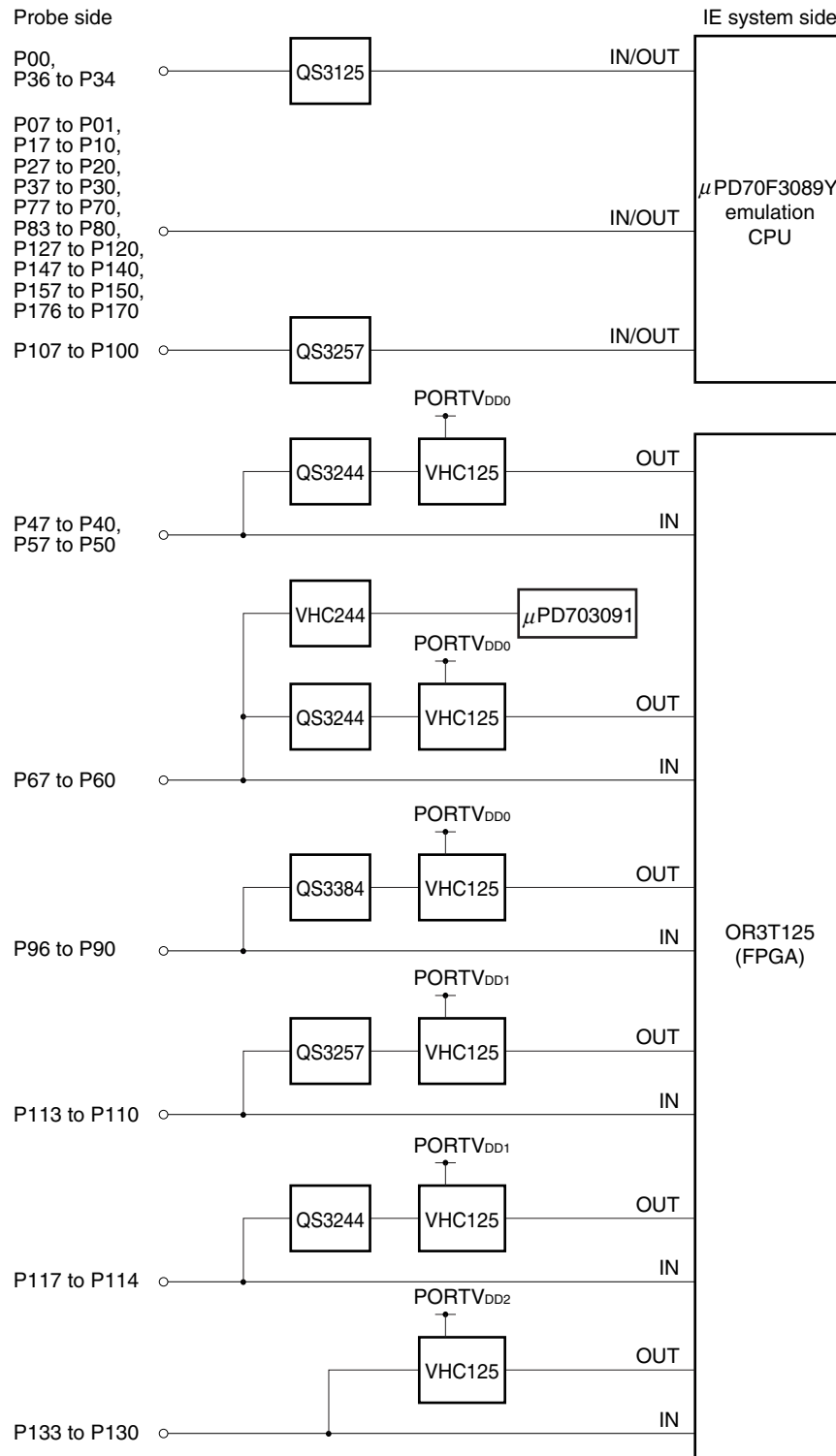
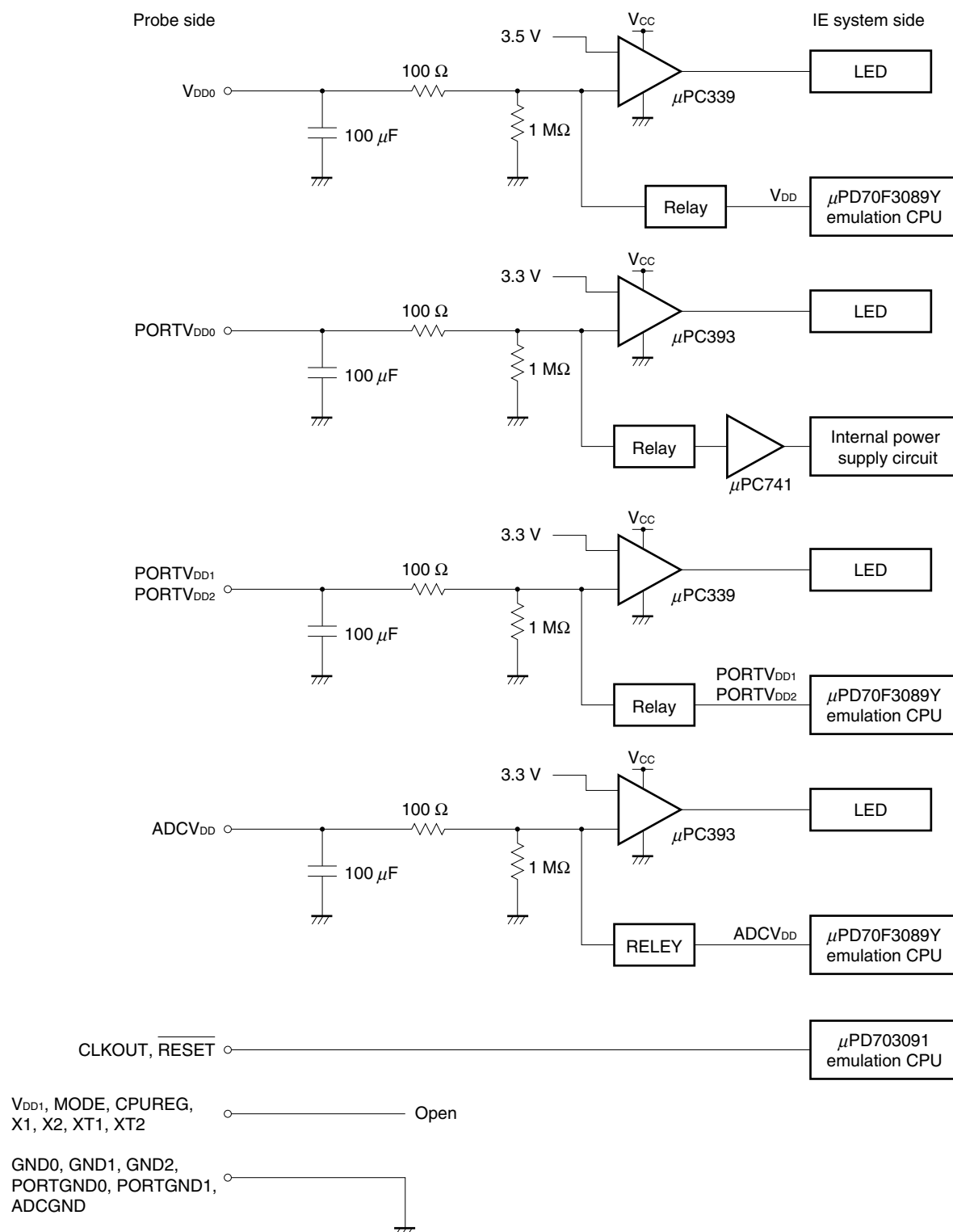
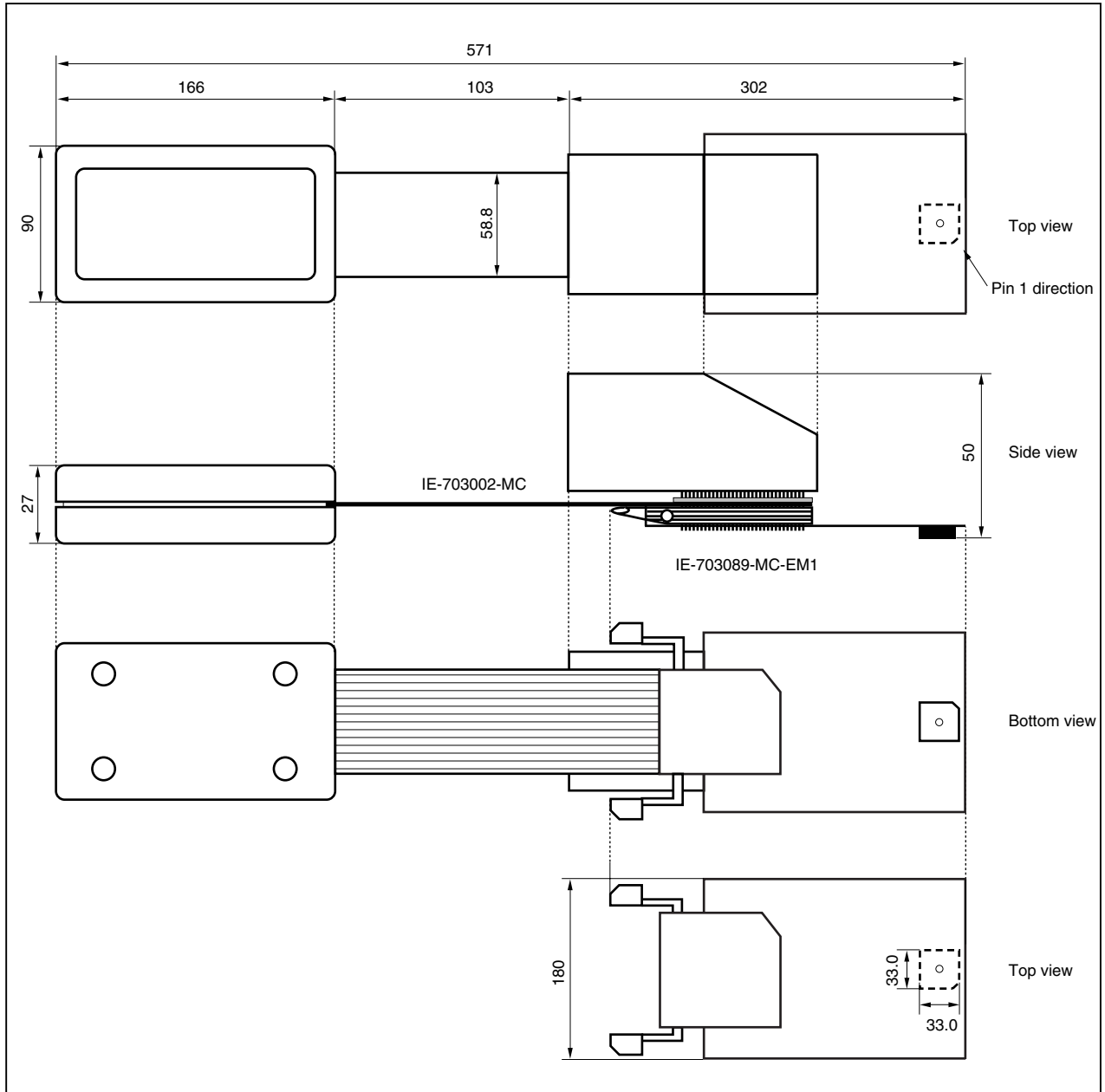


Figure 5-1. Equivalent Circuit of Emulation Circuit (2/2)



APPENDIX PACKAGE DRAWINGS

IE-703002-MC + IE-703089-MC-EM1 (Unit: mm)



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